ABSTRACT OF THE DISCLOSURE

A system and method for providing reset control between two integrated circuit domains (ICDs) disposed in a synchronous relationship. Upon reset, control signals are generated in a first ICD for resetting driver/receiver circuitry therein in a phased manner. An inter-ICD reset control signal is generated by the first ICD for transmission to the second ICD, wherein the inter-ICD reset control signal is operable to reset the second ICD's driver/receiver circuitry and other components therein.